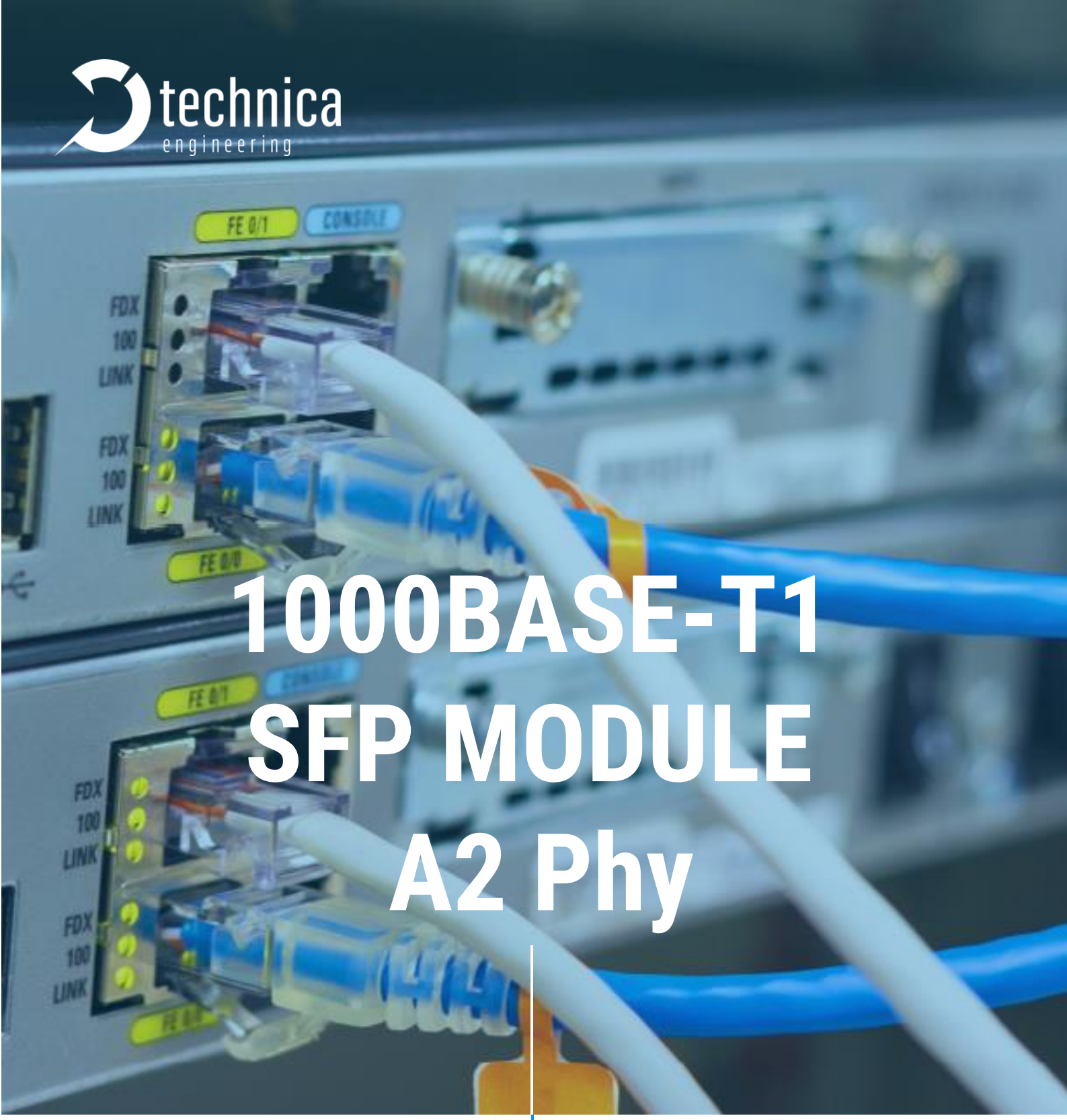
technica engineering



1000BASE-T1 SFP MODULE A2 Phy

USER MANUAL

September 2019

Manual-Version: 2.2

Hardware-Version: 2.3

CONTENT

1 GENERAL INFORMATION

1.1 Functionality and Features of the 1000BASE-T1 SFP Module A2 Phy

Figure 1-1: 1000BASE-T1 SFP Module A2 Phy

The **Technica Engineering 1000BASE-T1 SFP Module A2 PHY** fits into a standard Small Form-factor Pluggable slot
It uses the SGMII and generates 1000 Mbit/s full-duplex.

Note: SERDES interface is not supported!

After power up, it self-configures to Automotive 1000BASE-T1.
Registers of the integrated transceiver are accessible via I2C interface for diagnosis and reconfiguration.
One Link LED shows link status.

Features:

- 1000BASE-T1 and SGMII converter
- Marvell 88Q2112 A2 PHY (“IEEE Compliant” or “A0 compatible” mode settable via phy register settings)
- Fits into a standard SFP slot
- Power requirements: 3.3 Volt DC
- Supports I2C for internal register access
- Master/Slave either via small DIP switch or PHY register settings
- Status LEDs
- DIP switch for Master/ Slave configuration
-

General Information:

Power requirement:	3.3 Volt DC +/- 0.03 Volt
Power consumption:	Standard SFP compliant
Size:	68 x 14 x 14 mm
Weight:	0,1 kg
International Protection:	IP 2 0
Operating temperature:	0 to +70 °Celsius

LINKS:

The User can download the latest firmware and documentation for the 1000BASE-T1 SFP Module A2 PHY here:

https://technica-engineering.de/en/produkt/1000BASE-t1-sfp-module/

1.2 Warranty and Safety Information

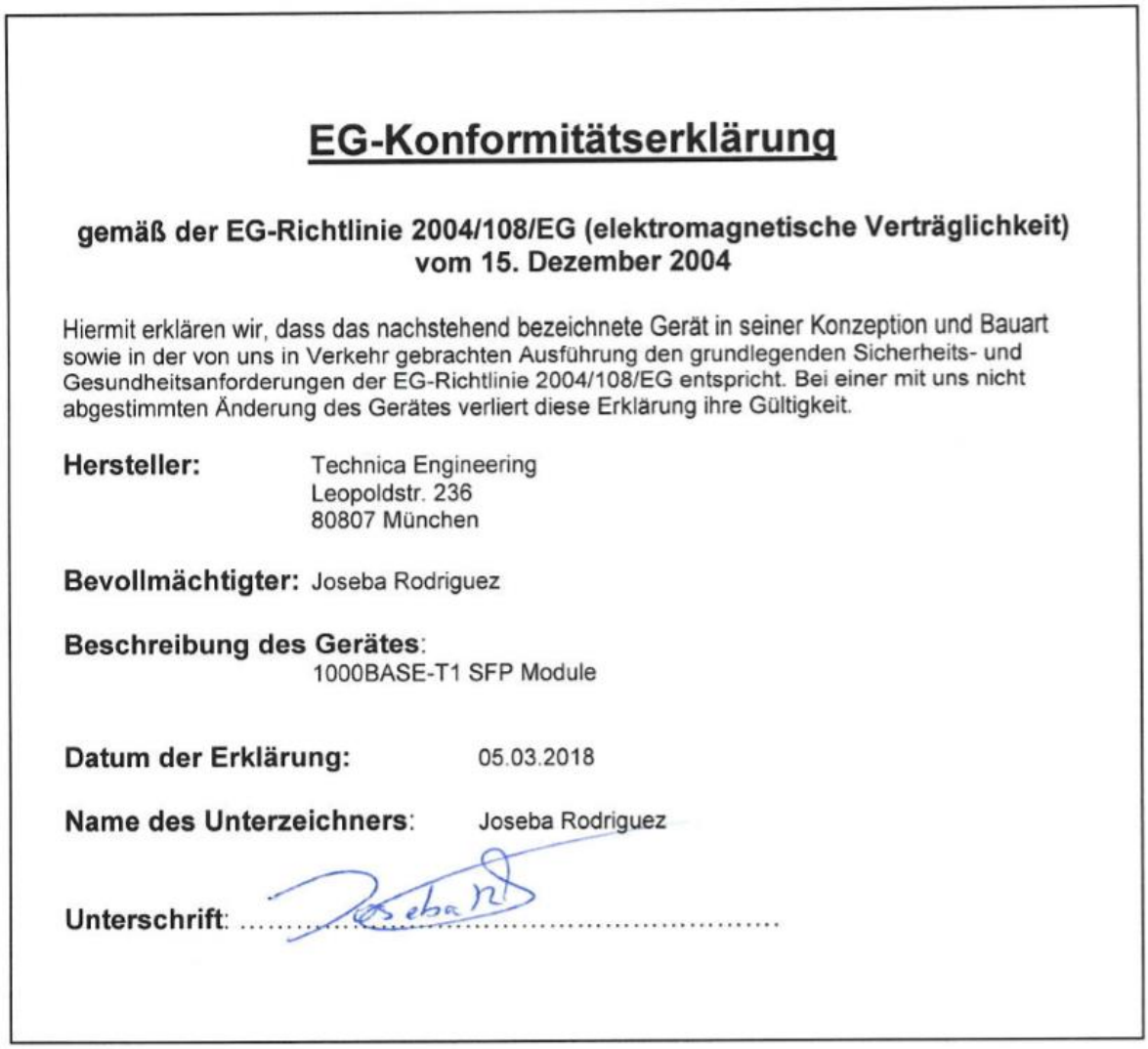
Before operating the device, read this manual thoroughly and retain it for your reference.
The latest documentation for the 1000BASE-T1 SFP Module A2 Phy can be downloaded here:
https://technica-engineering.de/en/produkt/1000BASE-t1-sfp-module/

Use the device only as described in this manual.
Use only in dry conditions.
Do not apply power to a damaged device.

Do not open the device. Otherwise warranty will be lost.

This device is designed for engineering purpose only.
Special care has to be taken for operation.
Do not use this device in a series production car.
As this device is likely to be used under rough conditions, warranty is limited to 1 year.
Manufacturer liability for damage caused by using the device is excluded.

1.3 Declaration of Conformity



EG-Konformitätserklärung

gemäß der EG-Richtlinie 2004/108/EG (elektromagnetische Verträglichkeit) vom 15. Dezember 2004

Hiermit erklären wir, dass das nachstehend bezeichnete Gerät in seiner Konzeption und Bauart sowie in der von uns in Verkehr gebrachten Ausführung den grundlegenden Sicherheits- und Gesundheitsanforderungen der EG-Richtlinie 2004/108/EG entspricht. Bei einer mit uns nicht abgestimmten Änderung des Gerätes verliert diese Erklärung ihre Gültigkeit.

Hersteller: Technica Engineering
Leopoldstr. 236
80807 München

Bevollmächtigter: Joseba Rodriguez

Beschreibung des Gerätes:
1000BASE-T1 SFP Module

Datum der Erklärung: 05.03.2018

Name des Unterzeichners: Joseba Rodriguez

Unterschrift: .....

Figure 1-2: Declaration of conformity

2 HARDWARE INTERFACES

2.1 Connector

The 1000BASE-T1 line is connected by a Molex connector.

Hardware Version 2.3. uses:

- Molex 0533250260 Header 2.0mm
- Molex 510900200 Housing
- Molex 50212-8000 Crimp Contact

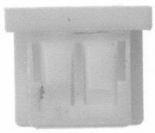
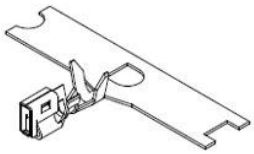
Name	Picture	Part Number
Molex Header 2.0mm		0533250260
Molex Housing		51090-0200
Molex 50212-8000 Crimp Contact		50212-8000

Table 2-1: Parts Molex Connector

Pinning:

Pin	Function	Pin	Function
1	1000BASE-T1 Plus	**2**	1000BASE-T1 Minus

Table 2-2: Pinning of Molex Connector

2.2 SFP Socket connector

SFP Socket connector:

Pin	Function	Pin	Function
1	GND	**11**	GND
2	GND	**12**	SGMII_RXD_N
3	n.c.	**13**	SGMII_RXD_P
4	I2C_DAT	**14**	GND
5	I2C_CLK	**15**	3.3 Volt
6	GND	**16**	3.3 Volt
7	n.c.	**17**	GND
8	GND	**18**	SGMII_TXD_P
9	n.c.	**19**	SGMII_TXD_N
10	GND	**20**	GND

Table 2-3: Pinning of black MQS connector

3 STARTUP AND CONFIGURATION

3.1 Startup

After 3.3 Volt power is applied, the SFP module starts up and self-configures the 88Q2112_A2 transceiver by MDIO interface. This lasts 100ms. Do not apply any I2C activity on the bus during this time!

3.2 Self-Configuration

The SFP Module configures itself to 1000BASE-T1 after power up. Master-/Slave Configuration is done according to the DIP switch on the bottom of the device.

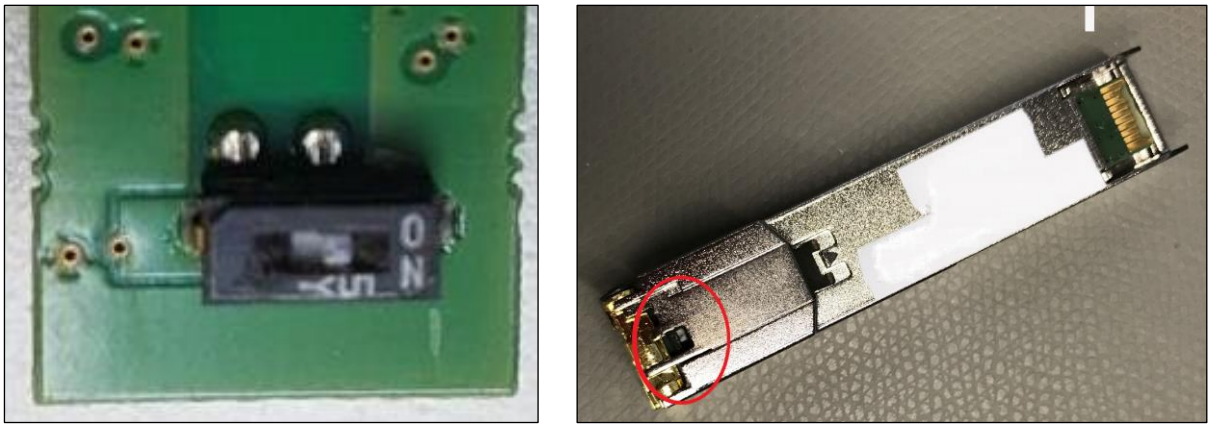


Figure 3-1: DIP-Switch

To reconfigure the DIP switch the lock has to be opened (see pictures).

ON/right = as Master
OFF/ left = as Slave

3.3 I2C Interface

3.3.1 I2C configuration

100ms after power up of the module it can be configured by I2C.

The module operates with f_{SCL} up to 53kHz without requiring clock stretching.
The module may clock stretch with f_{SCL} greater than 53kHz and up to 400 kHz.

The module processor listens as slave on the 7-bit address 0x50.
Note: b1010 000X = 0xA0
Read access beyond address 95 will return 0x00.

The 88Q2112_A2 transceiver can be accessed at I2C slave 7-bit address 0x40.
Note: b1000 000X = 0x80

The 88Q2112_A1 PHY does not support I2C interfaces. However, the microcontroller acts as a bridge between the host and the PHY. Commands from the Host are processed by the microcontroller. The microcontroller accesses to the PHY trough MDIO interface and forwards the information to the Host.
For a complete register map please have a look at the 88Q2112_A1 datasheet (NDA required).

3.3.2 I2C map register

Memory Map (read only registers):

Data Bytes	Byte Number	Comment
0x03	0	Identifier SFP
0x04	1	Ext. Identifier
0x80	2	Connector
0x00, 0x00, 0x00, 0x00	3-6	Transceiver high
0x00, 0x00, 0x00, 0x00	7-10	Transceiver low
0x00	11	Encoding
0x01	12	Bitrate Nominal in 100 MBit
0x00	13	Reserved
0x00	14	Link Length Fiber
0x00	15	Link Length Fiber
0x00	16	Link Length Fiber
0x00	17	Link Length Fiber
0x0A	18	Link Length Copper in meter
0x00	19	Reserved
'T','e','c','h','n','i','c','a',' ','E','n','g','.',' ',' ',' '	20-35	Vendor Name
0x00	36	Reserved
0x00, 0x00, 0x00	37-39	Vendor ID
'1','0','0','B','A','S','E','-','T','1',' ',' ',' ',' ',' ',' '	40-55	PartNumber
0x00, 0x00, 0x00, 0x00	56-59	Revision Number
0x00, 0x00, 0x00	60-62	Reserved
0xBC	63	Check Code for Field 0-62
0x00, 0x00	64-65	Options
0x00	66	Bitrate max
0x00	67	Bitrate min
0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00	68-83	Serial Number String
0x00, 0x00, 0x00, 0x00	84-87	Date Code high
0x00, 0x00, 0x00, 0x00	88-91	Date Code low
0x00, 0x00, 0x00	92-94	Reserved
0x42	95	Check Code Extended for Field 64-94

Table 3-1: Memory map

3.3.3 I2C Device addressing and operation

3.3.3.1 I2C Current address read

The current read operation only requires the device address read word to be sent. When the acknowledge is received from the SFP module, the current address data word is serially clocked out.

Example: Read the current address of the SFP module (b1010000X).

		<-I2C_device ->																		
HOST	START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	0	1	0	X	X	X	X	X	X	X	X	1	
SFP										ACK	MSB							LSB		
											<- DATA WORD->									

3.3.3.2 Random address read

The random address read requires two operations to perform the read.

Example: Read a random address of the SFP module (b1010000X)
First a write operation to specify the address desired to read:

		<-I2C_device ->									<-I2C Memory address->								
HOST	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X	0
SFP										ACK									ACK

Then a read operation to read the previous address specified:

		<-I2C_device ->																		
HOST	START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	0	1	0	X	X	X	X	X	X	X	X	1	
SFP										ACK	MSB							LSB		
											<- DATA WORD->									

3.3.3.3 Sequential read

The sequential reads are started by either a current word address read or a random address read. To specify a sequential read, the host responds with an acknowledge instead of a stop after each data word.

First a write operation to specify the address desired to read:

		<-I2C_device ->									<-I2C Memory address->								
HOST	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X	0
SFP										ACK									ACK

Then the read operations:

		<-I2C_device ->									<-DATA WORD n->									<-DATA WORD n+1->										
HOST	START	MSB						LSB	READ										ACK									NACK	STOP
		1	0	1	0	0	0	0	1	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	1	
SFP										ACK	MSB							LSB		MSB							LSB		

3.3.3.4 Byte Write

The write operation requires 8-bits of data word address following the device address write word and acknowledgement.

Example: Byte write operation into the SFP module (b1010000X)

		<-I2C_device ->									<-MEMORY ADDRESS->									<-DATA WORD->										
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0	
SPF										ACK									ACK									ACK	

3.3.3.5 Sequential write

The sequential write is started in the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in.

		<-I2C_device ->									<-MEMORY ADDRESS->									<-DATA WORD 1->									<-DATA WORD 2->										
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0	
SPF										ACK									ACK									ACK									ACK	

3.3.4 I2C access to the 88Q2112_A2 transceiver

The 88Q2112_A2 PHY listens as slave on the 7-bit address 0x40. Every internal register of the PHY (16 bits) is accessed by defining the Device Number (1 byte) and the Register address (2 bytes). The I2C Memory address is mapped as:

Address	Register name
0x00	Device number
0x01	Register_address_MSB
0x02	Register_address_LSB
0x03	PHY_Register_Operation_Status
0x04	PHY_Register_data_MSB
0x05	PHY_Register_data_LSB

Table 3-2: Register addresses

3.3.4.1 Register description

- **Device number:**
  Defines the device number of the register to access

- **Register_address_MSB:**
  Defines the Most significant byte of the register to access

- **Register_address_LSB:**
  Defines the Less Significant Byte of the register to access

- **PHY_Register_Operation_Status**

  - **Bit 0 – Read Start Condition Flag (Read/Write)**
    This flag is set by the master after specifying the first 3 bytes of the register (Devices number, Register_address_MSB and Register_address_LSB) when a read operation is trigged.

  - **Bit 1 – Read In Progress Flag (Read)**
    This flag is set by the slave during the reading operation

  - **Bit 2 – Read Operation Done Flag (Read)**
    This flag is set by the slave when the reading operation is finished. This flag can be read after triggering the read to ensure that the data has finished reading.

  - **Bit 3 – Write Start Condition Flag (Read)**
    This flag is set by the slave when a write operation is trigged.

- **Bit 4 – Write In Progress Flag (Read)**
  This flag is set by the slave during the writing operation

- **Bit 5 – Write Operation Done Flag (Read)**
  This flag is set by the slave when the writing operation is finished. This flag can be read after writing the PHY_register_data_LSB to ensure that the data has finished writing

- **PHY_register_data_MSB**
  When a reading operation, this register contains the MSB of the PHY register. When a write operation, this register contains the MSB to write in the PHY register

- **PHY_register_data_LSB**
  When a reading operation, this register contains the LSB of the PHY register. When a write operation, this register contains the LSB to write in the PHY register

4 ADDITIONAL INFORMATION

- The 1000BASE-T1 Port is optimized for automotive UseCase. The maximum line length for each 1000BASE-T1 segment is limited to 10 meters.

5 LIST OF FIGURES

6 CHANGELOG

Version	Chapter	Description	Date
1.0	All	First release	
2.0	All	Second release	21.09.2018
2.1.1	All	Design and correction of the bugs	05.03.2019
2.1.2	All	Control the User Manual of A2 Phy	08.05.2019
2.2	All	Rework	25.09.2019

7 CONTACT

If you have any questions regarding this product, please feel free to contact us:

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Most current user manuals and product information:
https://technica-engineering.de/